

wherein the second end portions are opposed to the first end portion in the second direction.

26. The device according to claim **21**, wherein the first selection transistor includes a gate electrode on the one of the first semiconductor layers, the gate electrode is covered with a second upper surface of the one of the first semiconductor layers and the first side surfaces of the one of the first semiconductor layers via a gate insulating layer.

27. The device according to claim **21**, further comprising: a second selection transistor disposed on one of the second semiconductor layers, wherein a gate electrode of the second selection transistor is electrically connected to a gate electrode of the first selection transistor, and

a first distance between a second upper surface of the one of the second semiconductor layers and a first under surface of the semiconductor substrate is equal to a second distance between a third upper surface of the one of the first semiconductor layers and the first under surface of the semiconductor substrate.

28. The device according to claim **27**, further comprising: an electrode layer extending in the third direction and disposed across the one of the first semiconductor layers and the one of the second semiconductor layers, wherein the electrode layer includes the gate electrode of the second selection transistor and the gate electrode of the first selection transistor.

29. The device according to claim **28**, wherein a portion of the electrode layer is disposed between the first side surface of the one of the first semiconductor layers and the second side surface of the one of the second semiconductor layers.

30. The device according to claim **21**, wherein: first end portions of the plurality of first layers have a stair shape.

31. The device according to claim **21**, further comprising: a peripheral circuit disposed on a second upper surface of a second part included in the semiconductor substrate,

wherein a first distance between the first upper surface and a first under surface of the semiconductor substrate is shorter than a second distance between the second upper surface and the first under surface.

32. The device according to claim **21**, wherein each of the first memory portions includes a memory layer disposed between the conductive layer and the first side surfaces.

33. The device according to claim **32**, wherein the memory layer is continuous between an under surface of the plurality of first layers and a second upper surface of the plurality of first layers in the first direction.

34. The device according to claim **32**, wherein the memory layer includes, a first insulating layer, a second insulating layer, and a charge storage layer between the first insulating layer and the second insulating layer,

the first insulating layer is disposed between the charge storage layer and the first side surfaces, and the second insulating layer is disposed between the charge storage layer and the conductive layer.

35. The device according to claim **32**, wherein the memory layer includes a chalcogenide layer.

36. The device according to claim **32**, wherein the memory layer includes a resistance change layer.

37. The device according to claim **21**, wherein the conductive layer extends in the first direction.

38. The device according to claim **21**, wherein a conductive layer is disposed between the first side surfaces and the second surfaces.

39. The device according to claim **21**, wherein the plurality of the first layers include first insulating layers,

wherein the first insulating layers and the first semiconductor layers are alternately stacked in the first direction.

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